

## WHAT IS CLAIMED IS:

1. A semiconductor device comprising:  
a device isolation layer disposed in a substrate to define an active region;  
5 source and drain regions formed in the active region;  
a gate electrode formed on the active region between the source and drain regions;  
a gate insulation layer interposed between the gate electrode and the active region;  
a resistor pattern formed on the device isolation layer; and  
resistor electrodes connected to both ends of the resistor pattern, respectively, wherein  
10 the gate electrode includes a polysilicon layer and a silicide layer that are sequentially stacked  
on the gate insulation layer, and wherein the resistor pattern includes a single polysilicon  
layer.
2. The device of claim 1, wherein the gate insulation layer is multi-layered and  
15 includes at least one silicon nitride layer.
3. The device of claim 1, wherein the resistor pattern is in direct contact with the  
device isolation layer.
- 20 4. The device of claim 1, wherein the resistor pattern includes a polysilicon layer  
with a hollow region where the device isolation layer is exposed and a region adjacent the  
hollow region is a single polysilicon layer.
- 25 5. The device of claim 4, further comprising:  
upper spacers formed on the polysilicon layer and including a vertical sidewall and a  
curved sidewall; and  
resistor spacers formed on outer sidewalls of the polysilicon layer and vertical  
sidewalls of the upper spacers, wherein the curved sidewall of the upper spacer is aligned to  
inner sidewalls of the polysilicon layer and the vertical sidewall thereof, opposite to the  
30 curved sidewall, is aligned to an outer sidewall of the polysilicon layer.
6. The device of claim 1, wherein the resistor pattern comprises:  
a line-shaped polysilicon pattern disposed on the device isolation layer; and

silicide patterns stacked on both ends of the polysilicon pattern, and wherein the resistor electrodes are connected to the silicide pattern.

5        7.        A method of fabricating a semiconductor device comprising:  
forming a device isolation layer in a substrate to define an active region;  
forming a gate pattern and a resistor pattern that include sequentially stacked first and  
second conductive layers on the active region and the device isolation layer, respectively;  
forming gate spacers and resistor spacers on sidewalls of the gate pattern and the  
resistor pattern, respectively;  
10        removing the second conductive layer of the resistor pattern to expose a portion of the  
inner sidewalls of the resistor spacers and a of the first conductive layer; and  
forming resistor electrodes connected to ends of the resistor pattern.

15        8.        The method of claim 7, further comprising patterning the exposed first  
conductive layer of the resistor pattern to expose the device isolation layer and form a hollow  
region surrounded by the first conductive layer.

20        9.        The method of claim 7, wherein the first conductive layer is formed of  
polysilicon and the second conductive layer is formed of silicide.

25        10.       A method of fabricating a semiconductor substrate comprising:  
forming a device isolation layer in a substrate to define an active region;  
stacking a polysilicon layer and a silicide layer on the entire surface of the substrate;  
patterning the polysilicon layer and the silicide layer to form a gate pattern of a first  
polysilicon pattern and a first silicide pattern on the active region, and to form a line-shaped  
resistor pattern of a second polysilicon pattern and a second silicide pattern on the device  
isolation layer;  
forming gate spacers and resistor spacers on sidewalls of the gate pattern and the  
resistor pattern, respectively;  
30        etching the second silicide pattern to expose a portion of inner sidewalls of the resistor  
spacers aligned to sidewalls of the second polysilicon pattern and a top of the second  
polysilicon pattern; and  
forming resistor electrodes connected to ends of the resistor pattern, respectively.

11. The method of claim 10, wherein the exposing the top of the second polysilicon pattern comprises:

forming a first interlayer dielectric layer with an opening exposing a top of the resistor pattern on an entire surface of the substrate;

5 etching the second silicide pattern of the exposed resistor pattern to expose a portion of inner sidewalls of the resistor spacers aligned to the sidewalls of the second polysilicon pattern and a top of the second polysilicon pattern; and

forming a second interlayer dielectric layer filling the opening, wherein the resistor electrode is formed to connect with the resistor pattern through the first and second interlayer dielectric layer.

12. The method of claim 10, after exposing the top of the second polysilicon pattern, further comprising forming an interlayer dielectric layer on an entire surface of the substrate, wherein the resistor electrodes are formed to connect with the resistor electrode through the interlayer dielectric layer.

13. The method of claim 10, wherein during the etching the second silicide pattern, the second silicide pattern remains at the ends of the resistor pattern.

20 14. A method of fabricating a semiconductor device comprising:  
forming a device isolation layer in a substrate to define an active region;  
stacking a polysilicon layer and a silicide layer on an entire surface of the substrate;  
patterning the polysilicon layer and the silicide layer to form a gate pattern  
comprising a first polysilicon pattern and a first silicide pattern on the active region, and to  
25 form a line-shaped resistor pattern comprising a second polysilicon pattern and a second silicide pattern on the device isolation layer;

forming gate spacers and resistor spacers on sidewalls of the gate pattern and the resistor pattern, respectively;

30 etching the second silicide pattern of the resistor pattern to expose a portion of the inner sidewalls of the resistor pattern aligned to sidewalls of the second polysilicon pattern and a top of the second polysilicon pattern;

forming upper spacers including a vertical sidewall aligned to the inner sidewall of the resistor spacers and a curved sidewall opposite to the vertical sidewall, on the inner sidewalls of the exposed resistor spacers on the exposed second polysilicon pattern;

using the upper spacers as an etch mask, etching the second polysilicon pattern to form a hollow region where the device isolation layer is exposed, wherein the hollow region includes sidewalls aligned to the curved sidewalls of the upper spacers; and forming resistor electrodes connected to both edges of the resistor pattern.

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15. The method of claim 14, wherein the exposing the top of the second polysilicon pattern comprises:

forming a first interlayer dielectric layer with an opening exposing a top of the resistor pattern on the entire surface of the substrate; and

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etching the second silicide pattern of the exposed resistor pattern to expose a portion of inner sidewalls of the resistor spacers aligned to sidewalls of the second polysilicon pattern and the top of the second polysilicon pattern.

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16. The method of claim 15, wherein during forming the first interlayer dielectric layer, the first interlayer dielectric layer is formed to cover a portion of both edges of the resistor pattern.

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17. The method of claim 15, wherein during forming the first interlayer dielectric layer, the opening of the first interlayer dielectric layer is formed to expose an entire top surface of the resistor pattern.

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18. The method of claim 15, after forming the hollow region, further comprising forming a second interlayer dielectric layer filling the opening, wherein the resistor electrodes are formed to connect with the resistor pattern through the first and second interlayer dielectric layers.

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19. The method of claim 14, after forming the hollow region, further comprising forming the interlayer dielectric layer on an entire surface, wherein the resistor electrodes are formed to connect with the resistor pattern through the interlayer dielectric layer.

20. The method of claim 14, wherein during etching the second silicide pattern, the second silicide pattern remains at both edges of the resistor pattern.